9981954 Deepak Metha

EAST SEARCH

1/12/06

L#	Hits	Search String	Databases
S1	2	6,282,131.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	14	(memory near2 compiler$1) with (memory near2 instance$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	0	(memory near2 compiler$1) with charcaterization	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	10	(memory near2 instance$1) with compilable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	81	(memory near2 instance$1) with (parameter$1 or parametric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	1628	(memory near2 instance$1) with ((data near2 point$1) or data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	22	(memory near2 compiler$1) with (parameter$1 or parametric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	198	(memory near2 compiler$1) with ((data near2 point$1) or data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	1880	S2 or S4 or S5 or S6 or S7 or S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	1	S9 and (memory with (MUX near2 factor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	1	S9 and (MUX near2 factor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	2	S9 and (memory with ((parametric near2 dataset$1) or dataset$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	0	S9 and (congruent near2 (memory near2 instance$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	0	S9 and (congruent with (memory near2 instance$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	16	S9 and (scale near2 factor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	0	S9 and ((scale near2 factor$1) near2 interpolat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	109	S9 and (memory near2 timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	250	S9 and (memory with ((access or cycle) near2 time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	37	S17 and S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	0	S9 and (MUX-4 or MUX-8 or MUX-16 or MUX-32)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	176	S9 and ((memory near2 instance$1) with (ROM or ((static or dynamic) near2 RAM) or EPROM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	4	S9 and ((scale near2 factor$1) with interpolat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	22	S17 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	14	S18 and S21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	5	S9 and ((memory near2 compiler$1) with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	4	S9 and ((memory near2 compiler$1) with technolog$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	1	S9 and ((memory with technolog$3) with ("1.0" or "0.8" or "0.6" or "0.2"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	44	S9 and ((design near2 rule$1) or foundry-specific or rule-specific or process-specific or proces	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	150	S10 or S11 or S12 or S15 or S19 or S22 or S23 or S24 or S25 or S26 or S27 or S28 or S2 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	2	(memory near2 compiler$1) with characterization	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	14	(memory near2 compiler$1) with (memory near2 instance$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	10	(memory near2 instance$1) with compilable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	81	(memory near2 instance$1) with (parameter$1 or parametric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	1628	(memory near2 instance$1) with ((data near2 point$1) or data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	22	(memory near2 compiler$1) with (parameter$1 or parametric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	198	(memory near2 compiler$1) with ((data near2 point$1) or data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S37	1880	S31 or S32 or S33 or S34 or S35 or S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	1	S37 and (memory with (MUX near2 factor$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	1	S37 and (MUX near2 factor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	2	S37 and (memory with ((parametric near2 dataset$1) or dataset$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	16	S37 and (scale near2 factor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	109	S37 and (memory near2 timing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	250	S37 and (memory with ((access or cycle) near2 time))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	37	S42 and S43	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	176	S37 and ((memory near2 instance$1) with (ROM or ((static or dynamic) near2 RAM) or EPROI	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	4	S37 and ((scale near2 factor$1) with interpolat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	22	S42 and S45	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	14	S43 and S45	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	5	S37 and ((memory near2 compiler$1) with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	4	S37 and ((memory near2 compiler$1) with technolog$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	1	S37 and ((memory with technolog$3) with ("1.0" or "0.8" or "0.6" or "0.2"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	44	S37 and ((design near2 rule$1) or foundry-specific or rule-specific or process-specific or proce	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	6324	(memory near2 characteriz$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	44	S54 and (memory near2 compiler$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	248	S54 and (memory near2 instance$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	286	S55 or S56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	1	S37 and (multiplex$3 near2 factor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	2	S57 and (multiplex$3 near2 factor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	37	S37 and (memory with ("1.0" or "0.8" or "0.6" or "0.2"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	18	S57 and (memory with ("1.0" or "0.8" or "0.6" or "0.2"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	6	S55 and S56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	98	S55 or S58 or S59 or S60 or S61 or S62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	150	S38 or S39 or S40 or S41 or S44 or S46 or S47 or S48 or S49 or S50 or S51 or S52 or S31 o	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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Results of search set S63

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20050114560	A1	Tightly coupled and scalable memory and execution unit architecture	20050526	710/22	
US 20050108398	A1	Systems and methods for using metrics to control throttling and swapping in a message proce:	20050519	709/225	
US 20050102472	A1	Data processor having cache memory	20050512	711/120	
US 20050060500	A1	General purpose memory compiler system and associated methods	20050317	711/147	
US 20050055675	A1	Generation of software objects from a hardware description	20050310	717/135	
US 20050047238	A1	Reconfigurable memory arrays	20050303	365/210	
US 20050039156	A1	Design method for essentially digital systems and components thereof and essentially digital s	20050217	716/18	
US 20040215893	A1	Method for use of ternary cam to implement software programmable cache policies	20041028	711/138	
US 20040205290	A1	Memory device	20041014	711/103	

US 20040202025 A1	Nonvolatile semiconductor memory device	20041014	365/185.29
US 20040202019 A1	Nonvolatile semiconductor memory device	20041014	365/185.01
US 20040196712 A1	Semiconductor memory device	20041007	365/202
US 20040151038 A1	Memory module and method for operating a memory module in a data memory system	20040805	365/200
US 20040122644 A1	Optimized execution of software objects generated from a hardware description	20040624	703/16
US 20040117168 A1	Global analysis of software objects generated from a hardware description	20040617	703/14
US 20040117167 A1	Simulation of software objects generated from a hardware description	20040617	703/14
US 20040111690 A1	Method for composing memory on programmable platform devices to meet varied memory re	20040610	716/17
US 20040088702 A1	Lock-free overflow strategy for work stealing	20040506	718/100
US 20040071009 A1	Compilable address magnitude comparator for memory array self-testing	20040415	365/145
US 20040036700 A1	Data communications device, data communications system, document display method with vid	20040226	345/660
US 20040015925 A1	Method, article of manufacture and apparatus for performing automatic intermodule call linkage	20040122	717/155
US 20030225740 A1	Memory model for a run-time environment	20031204	707/1
US 20030204676 A1	Data processor having cache memory	20031030	711/137
US 20030192013 A1	Method and apparatus for facilitating process-compliant layout optimization	20031009	716/2
US 20030178648 A1	Gate array core cell for VLSI ASIC devices	20030925	257/202
US 20030156751 A1	Method of and apparatus for rectifying a stereoscopic image	20030821	382/154
US 20030105772 A1	Write-barrier maintenance in a garbage collector	20030605	707/103R
US 20030103379 A1	Semiconductor memory device	20030605	365/185.2
US 20030026131 A1	Redundancy circuit and method for replacing defective memory cells in a flash memory device	20030206	365/185.11
US 20030026129 A1	REDUNDANCY CIRCUIT AND METHOD FOR FLASH MEMORY DEVICES	20030206	365/185.09
US 20030002347 A1	Nonvolatile semiconductor memory device	20030102	365/185.29
US 20020191448 A1	Timing circuit and method for a compilable dram	20021219	365/194
US 20020176282 A1	Nonvolatile semiconductor memory device	20021128	365/185.22
US 20020154553 A1	System and method for redundancy implementation in a semiconductor device	20021024	365/200
US 20020131320 A1	SRAM emulator	20020919	365/233
US 20020083262 A1	MEMORY DEVICE OPERABLE WITH A SMALL-CAPACITY BUFFER MEMORY AND HAVIN	20020627	711/103
US 20020046251 A1	Streaming memory controller	20020418	709/213
US 20020042897 A1	Method and system for distributed testing of electronic devices	20020411	714/718
US 20020035671 A1	Processor with cache control	20020321	711/118
US 20020013881 A1	Dynamically-tunable memory controller	20020131	711/105
US 20010048610 A1	Semiconductor memory device	20011206	365/185.2
US 20010037432 A1	Data processor having cache memory	20011101	711/129
US 20010030889 A1	Nonvolatile semiconductor memory device	20011018	365/185.05
US 20010014933 A1	Memory management table producing method and memory device	20010816	711/154
US 6895452 B1	Tightly coupled and scalable memory and execution unit architecture	20050517	710/22
US 6892328 B2	Method and system for distributed testing of electronic devices	20050510	714/42
US 6853572 B1	Methods and apparatuses for a ROM memory array having twisted source or bit lines	20050208	365/63
US 6850446 B1	Memory cell sensing with low noise generation	20050201	365/206
US 6848027 B2	Data processor having cache memory	20050125	711/129
US 6842375 B1	Methods and apparatuses for maintaining information stored in a non-volatile memory cell	20050111	365/185.18
US 6836831 B2	Independent sequencers in a DRAM control structure	20041228	711/169
US 6791882 B2	Nonvolatile semiconductor memory device	20040914	365/185.29

US 6788574 B1	Electrically-alterable non-volatile memory cell	20040907	365/185.08
US 6765245 B2	Gate array core cell for VLSI ASIC devices	20040720	257/202
US 6747902 B2	Nonvolatile semiconductor memory apparatus	20040608	365/185.29
US 6745372 B2	Method and apparatus for facilitating process-compliant layout optimization	20040601	716/2
US 6738953 B1	System and method for memory characterization	20040518	716/1
US 6735120 B2	Semiconductor device having a high-speed data read operation	20040511	365/185.2
US 6711092 B1	Semiconductor memory with multiple timing loops	20040323	365/233
US 6704834 B1	Memory with vectorial access	20040309	711/5
US 6678643 B1	Event based semiconductor test system	20040113	703/14
US 6658610 B1	Compilable address magnitude comparator for memory array self-testing	20031202	714/718
US 6647465 B2	Realtime parallel processor system for transferring common information among parallel proces	20031111	711/131
US 6625712 B2	Memory management table producing method and memory device	20030923	711/202
US 6598190 B1	Memory device generator for generating memory devices with redundancy	20030722	714/711
US 6597629 B1	Built-in precision shutdown apparatus for effectuating self-referenced access timing scheme	20030722	365/233
US 6594177 B2	Redundancy circuit and method for replacing defective memory cells in a flash memory device	20030715	365/185.11
US 6587927 B2	Data processor having cache memory	20030701	711/129
US 6587364 B1	System and method for increasing performance in a compilable read-only memory (ROM)	20030701	365/63
US 6584036 B2	SRAM emulator	20030624	365/233
US 6578129 B1	Optimized virtual memory management for dynamic data types	20030610	711/209
US 6563732 B2	Redundancy circuit and method for flash memory devices	20030513	365/185.09
US 6556490 B2	System and method for redundancy implementation in a semiconductor device	20030429	365/200
US 6538932 B2	Timing circuit and method for a compilable DRAM	20030325	365/194
US 6532174 B2	Semiconductor memory device having high speed data read operation	20030311	365/185.2
US 6473356 B1	Low power read circuitry for a memory circuit based on charge redistribution between bitlines a	20021029	365/230.03
US 6466504 B1	Compilable block clear mechanism on per I/O basis for high-speed memory	20021015	365/218
US 6453434 B2	Dynamically-tunable memory controller	20020917	714/718
US 6438670 B1	Memory controller with programmable delay counter for tuning performance based on timing p:	20020820	711/167
US 6438036 B2	Nonvolatile semiconductor memory device	20020820	365/185.22
US 6434658 B1	Memory device operable with a small-capacity buffer memory and having a flash memory	20020813	711/103
US 6425116 B1	Automated design of digital signal processing integrated circuit	20020723	716/18
US 6425062 B1	Controlling burst sequence in synchronous memories	20020723	711/167
US 6424556 B1	System and method for increasing performance in a compilable read-only memory (ROM)	20020723	365/63
US 6405160 B1	Memory compiler interface and methodology	20020611	703/24
US 6370078 B1	Way to compensate the effect of coupling between bitlines in a multi-port memories	20020409	365/230.05
US 6363020 B1	Architecture with multi-instance redundancy implementation	20020326	365/200
US 6356503 B1	Reduced latency row selection circuit and method	20020312	365/230.06
US 6348774 B1	Method for controlling several stepping motor modules with prior loading of ramp data	20020219	318/685
US 6334174 B1	Dynamically-tunable memory controller	20011225	711/167
US 6292427 B1	Hierarchical sense amp and write driver circuitry for compilable memory	20010918	365/230.03
US 6282131 B1	Self-timed clock circuitry in a multi-bank memory instance using a common timing synchronizat	20010828	365/191
US 6275902 B1	Data processor with variable types of cache memories and a controller for selecting a cache m	20010814	711/129
US 6259629 B1	Nonvolatile semiconductor memory device	20010710	365/185.22
US 6249901 B1	Memory characterization system	20010619	716/5

US 6249471 B1	Fast full signal differential output path circuit for high-speed memory	20010619	365/207
US 6236618 B1	Centrally decoded divided wordline (DWL) memory architecture	20010522	365/230.06
US 6233197 B1	Multi-port semiconductor memory and compiler having capacitance compensation	20010515	365/230.05
US 6216180 B1	Method and apparatus for a nonvolatile memory interface for burst read operations	20010410	710/35
US 6181600 B1	Nonvolatile semiconductor memory device	20010130	365/185.18
US 6157576 A	Nonvolatile semiconductor memory device	20001205	365/185.29
US 6016273 A	Nonvolatile semiconductor memory device	20000118	365/185.22
US 6000522 A	Multi-compartment and acceptors computerized vending machine	19991214	194/217
US 5991200 A	Nonvolatile semiconductor memory device	19991123	365/185.18
US 5970986 A	Apparatus for rejection diagnostics after organ transplants	19991026	128/899
US 5970240 A	Method and apparatus for configurable memory emulation	19991019	703/25
US 5959894 A	Nonvolatile semiconductor memory device	19990928	365/185.29
US 5949715 A	Nonvolatile semiconductor memory device	19990907	365/185.22
US 5923610 A	Timing scheme for memory arrays	19990713	365/230.08
US 5917752 A	Nonvolatile semiconductor memory device	19990629	365/185.18
US 5848432 A	Data processor with variable types of cache memories	19981208	711/131
US 5844842 A	Nonvolatile semiconductor memory device	19981201	365/185.24
US 5808900 A	Memory having direct strap connection to power supply	19980915	716/10
US 5781732 A	Framework for constructing shared documents that can be collaboratively accessed by multipl	19980714	709/205
US 5781476 A	Nonvolatile semiconductor memory device	19980714	365/185.22
US 5644753 A	Fast, dual ported cache controller for data processors in a packet switched cache coherent mu	19970701	711/131
US 5640349 A	Flash memory system	19970617	365/185.33
US 5634107 A	Data processor and method of processing data in parallel	19970527	711/111
US 5555555 A	Apparatus which detects lines approximating an image by repeatedly narrowing an area of the	19960910	382/104
US 5528552 A	Dynamic random access memory device with sense amplifiers serving as cache memory inde	19960618	365/238.5
US 5493507 A	Digital circuit design assist system for designing hardware units and software units in a desired	19960220	703/14
US 5479374 A	Semiconductor memory device employing sense amplifier control circuit and word line control c	19951226	365/233.5
US 5479184 A	Videotex terminal system using CRT display and binary-type LCD display	19951226	345/3.1
US 5452226 A	Rule structure for insertion of new elements in a circuit design synthesis procedure	19950919	716/18
US 5400267 A	Local in-device memory feature for electrically powered medical equipment	19950321	702/59
US 5399912 A	Hold-type latch circuit with increased margin in the feedback timing and a memory device using	19950321	327/94
US 5222029 A	Bitwise implementation mechanism for a circuit design synthesis procedure	19930622	716/18
US 5175707 A	Semiconductor memory device having a driving circuit provided in association with a high spee	19921229	365/230.06
US 5050091 A	Integrated electric design system with automatic constraint satisfaction	19910917	716/10
US 5046113 A	Method of and apparatus for detecting pattern defects by means of a plurality of inspecting unit	19910903	382/147
US 4945495 A	Image memory write control apparatus and texture mapping apparatus	19900731	345/552
US 4875192 A	Semiconductor memory with an improved nibble mode arrangement	19891017	365/193
US 4845640 A	High-speed dual mode graphics memory	19890704	345/572
US 4803476 A	Video terminal for use in graphics and alphanumeric applications	19890207	345/545
US 4688182 A	Method and apparatus for generating a set of signals representing a curve	19870818	345/442
US 4686636 A	Method and apparatus for generating a set of signals representing a curve	19870811	345/442
US 4686634 A	Method and apparatus for generating a set of signals representing a curve	19870811	345/442
US 4686633 A	Method and apparatus for generating a set of signals representing a curve	19870811	345/442

US 4465349 A	Microfilm card and a microfilm reader with automatic stage positioning	19840814	353/25
US 4431007 A	Referenced real-time ultrasonic image display	19840214	600/440
US 4314331 A	Cache unit information replacement apparatus	19820202	711/133
US 4245304 A	Cache arrangement utilizing a split cycle mode of operation	19810113	711/122
US 4208716 A	Cache arrangement for performing simultaneous read/write operations	19800617	711/3
EP 647900 A1	Parameter storage space allocation.	19950412	
US 20050060500 A	Memory compiler units accessing method for generating memory related design files, involves	20050317	
US 6738953 B	Memory e.g. ROM characterization method, involves creating hierarchically-stitched parametric	20040518	
US 6282131 B	Timing synchronization method in memory instance, involves enabling address signals for subs	20010828	
US 6249901 B	Automatic memory characterization for designing integrated circuit, involves simulating circuit b	20010619	
EP 191134 A	Display data encoding of signals representing curve - using parametric cubic polynomial functic	19860820	
EP 175179 A	Signal generation method for points on curve - using compiler in form of Hermite cubic parame	19860326	